

What is claimed is:

1. A method for fabricating nanometer gate semiconductor device using thermally reflowed photoresist technology, comprising the following steps:

(i) spin-coating two layers of photoresists on a substrate, where a bottom layer of photoresist, one of said two layers of photoresists, is a polymeric photoresist which has a lower sensitivity and a higher resolution with respect to an electron beam, and a top layer of photoresist, one of said two layers of photoresists, is another polymeric photoresist which has a higher sensitivity and a lower resolution with respect to the electron beam;

(ii) heating said two layers of photoresists for curing by way of using a hotplate;

(iii) using photolithography with a high accelerating voltage in an electron beam direct writing manner to expose a pattern on said two layers of photoresists for forming a gate;

(iv) using a developer and an etchant for developing and etching in order to form a recess on the gate;

(v) plating a metallic layer on the recess of the gate by way of using an electron gun evaporation technique; and

(vi) removing said photoresists to obtain the gate, characterized in that after the etching of the recess of the gate, the photoresists are reflowed by using a hot plate heating manner within a predetermined period of time and temperature, such that the recess of the gate is formed with a nanometer-sized width.

2. The method according to Claim 1, wherein said bottom layer of photoresist is a PMMA (polymethyl methacrylate) photoresist or a LOR (lift-off) photoresist.

3. The method according to Claim 1, wherein said top layer of photoresist is a P(MMA-MAA) (poly (methacrylate-methyl acrylic acid)) photoresist or a PMGI (polymethylglutarimide) photoresist.

4. The method according to Claim 1, wherein said metallic layer is a Ti/Pt/Au Schottky metallic layer.

5. The method according to Claim 1, wherein said predetermined period of time and temperature for the reflow of said photoresists are 75 seconds and 125 °C, respectively, and the heating manner employs a bottom heating manner.

6. The method according to Claim 1, wherein the heating temperatures for the bottom and top layers of said photoresists are 250 °C and 180 °C, respectively, and the heating time of each layer is 3 minutes.
7. The method according to Claim 1, wherein said step of removing the photoresists employs acetone to remove said photoresists.
8. The method according to Claim 1, wherein the recess of the gate is T-shaped.
9. The method according to Claim 1, wherein said substrate is a GaAs substrate.
10. The method according to Claim 1, wherein said developer is a MIBK: IPA = 1 : 3 high resolution developer.
11. The method according to Claim 1, wherein said photoresists are at least two layers of multi-layered photoresists structure containing PMMA, LOR, PMGI, and P(MMA-MAA).